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FORMAL DEFINITION AND PROPERTIES OF FEB-BASED ENOB OF INTELLIGENT CYCLIC ADC

The paper presents a new approach to the measurement of effective resolution (effective number of bits – ENOB) of the cyclic A/D converters (CADCs). The core idea of the approach is a direct measurement of ENOB using, as a numerical measure, the number of true bits before the first erroneous bit (FEB) in the code of the sample. The position of FEB is determined by the first non-zero bit in the binary presentation of the conversion error. The FEB-based definition of ENOB is introduced and discussed. The results of simulation evaluations of FEB distributions in sequential cycles of conversion are presented and values of FEB-based ENOB are compared with the conventional ENOB evaluations. The influence of DNL and INL errors of internal A/D converter on directly and conventionally measured values of ENOB is analysed. The proposed method of ENOB measurement is less dependent on the class of the testing signal and can be used for more adequate assessment of actual ADC resolution.

Keywords: A/D resolution, ENOB, intelligent cyclic A/D converters

1. INTRODUCTION

Until now, a lot of difficulties remain in definition and unification of the measures of A/D conversion quality, as well as in methods of their measurement [1-3]. The main reason is a plural non-linearity of the ADC transition function of an which violates the principle of superposition enabling accurate formulation of these measures for linear systems. In this case, harmonic analysis cannot ensure repeatable and adequate results for the assessment of ADC performance. Each performance characteristics measured using the harmonic technique does not guarantee a corresponding quality of conversion with the ADC applied to different classes of signals. The results of a practical measurement depend on the form of input signals, and the actual resolution of the converter may differ from the resolution obtained in the tests.

This fact radically complicates the development of adequate and commonly accepted methods of ADC testing, quality analysis and comparison of characteristics.

This caused the appearance of a slowly but permanently growing number of different methods of ADC performance analysis and measures of quality, each having own right to be used and describing a particular aspect of ADC performance. (ENOB, SINAD, THD, SFDR, SNHR, INL, DNL, etc., see IEEE Standard 1241-2000 [1]). Designers and users of *cyclic* ADCs (CADCs) [3] and intelligent cyclic ADC (IC ADC, [4-10] and other works) encounter additional problems with the performance assessment.

The general architecture of a CADC is presented in Fig. 1. It is assumed that the input signals $V(t)$ (further, to shorten formulas, denoted as V_t) are stationary zero-mean Gaussian random processes with the variance not greater than given σ_0^2. The spectral power density is assumed to have zero values outside the frequency range [-F, F]. The sample-and-hold unit (S&H in Fig. 1) forms and holds the samples $V^{(m)} = V(m/2F)$, ($m = 1, 2, \ldots, M$), at the first input of subtracting block Σ each during the same time $T = 1/2F$. Each sample $V^{(m)} = V(m/2F)$ is converted independently in $n = F_0/2F$ cycles (F_0 is the band-pass of the analogue part of the converter). The latter permits to reduce the analysis of CADC work to the consideration of conversion of a single sample $V^{(m)} = V$. We assume also that the internal coarse "pre"-converter (ADC_{In}) has an ideal transfer function (no DNL, no INL), and the feedback D/A converter DAC_{In} has sufficiently high resolution permitting to consider the analogue signals $\hat{V}_k^{DAC}$ at the DAC_{In} output as numerically equal to the digital codes $\hat{V}_k$ at its input.

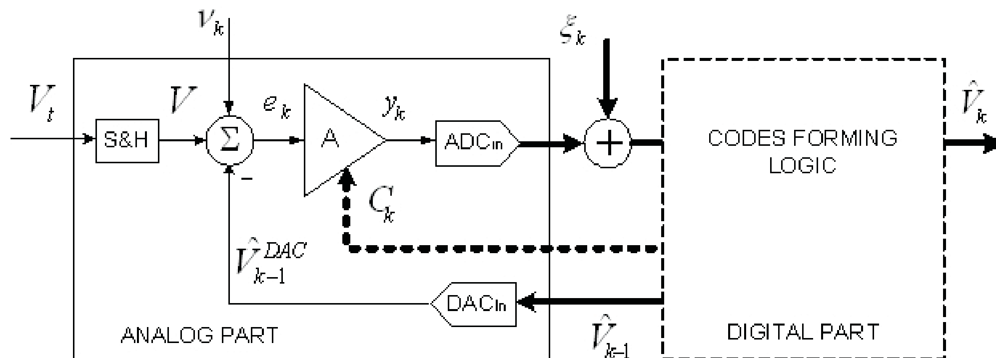

Fig. 1. General block-diagram of CADC.

Nowadays, in the performance measurements, CADCs are considered as the "black-boxes" and their characteristics are measured the same way and using the same measures of quality as those of the non-cyclic ADCs [1]. However, our investigations ([4-8] and others) have shown that this approach cannot be applied to IC ADC. Particularities of IC ADC operation do not allow to apply Standard [1] definitions and methods, which should be corrected taking into account the following factors established in our research:

1. The probability density function (PDF) of quantization noise at the IC ADC output is not uniform. The reason is low resolution of the coarse (N_{ADC} = 1-6 bit) internal ADC_{In} that makes its quantization noise ξ_k and final errors of conversion (IC ADC quantization noise) significantly non-uniform. For a greater number of cycles, the PDF of output quantization errors takes the Gaussian form [4, 5, 7, 8].
2. Both in IC ADC and CADC, influence of the testing signal characteristics (form, dynamic range, correlations, statistics and dynamics of changes) on the conversion quality practically disappears beginning with the second cycle of conversion. This is conditioned by approximate orthogonality of the residual signals $e_k = V - V_{k-1}^{DAC} + \nu_k$ routed to the input of amplifier (A) in the analogue part in sequential cycles $k = 1, \ldots, n$, ($\boldsymbol{n}$ is the last cycle of the sample conversion, $\boldsymbol{\nu_k}$ denotes the summary noise acting at the amplifier A input).
3. The probability of overloading of CADC and IC ADC grows, in sequential cycles, due to the increasing role of non-ideality of characteristics and internal noise in the analogue part of converters (the greater $\boldsymbol{k}$ the smaller SNR $\boldsymbol{E[V - \hat{V}_{k-1}]^2]/\sigma_\nu^2}$). Also, these factors increase the probability of errors in lower bits in the code words ("observations") $\tilde{\boldsymbol{y}}_{\boldsymbol{k}}$ at $\mathbf{ADC_{In}}$ output ("observations").

In the paper, the main attention is paid to the problem of formulation of adequate, clear and convenient for practical applications measures of IC ADC (and CADC) performance, as well as methods of their measurement. This task is especially actual for current research in the field of the new "intelligent" converters theory and design ([4-10] and other works). The concept of intelligent conversion is based on transformation and optimization of CADC architecture and parameters in the way making its performance approach the theoretical limit. This makes the problem of adequate and accurate measurements of their characteristics a key factor for successful development of the direction. Having no reliable tool for verification of the efficiency of new analytical and technical solutions one can neither assess nor confirm the advantages of "intelligent" CADC over their conventional prototypes.

The paper discusses the most convenient, clear, adequate and universal measure of conversion quality – the effective number of bits (ENOB) of a CADC. The research develops the "FEB-based ENOB" formulation enabling its direct measurement, omitting preliminary evaluation of RMS (root-mean-square error) of conversion, peculiar to known definitions of ENOB. In the final part of the paper, the dependence of FEB-based ENOB on the differential and integral non-linearities (DNL and INL, respectively) of the internal ADC_{In} is discussed and compared with similar results for the ENOB measured by conventional methods [9].

It is worth to say that elaboration of clear and adequate measures and methods of IC ADC performance analysis and testing will help to order the performance analysis and testing of other classes of ADCs.

2. DIFFERENCES BETWEEN INTELLIGENT AND CONVENTIONAL CADC

Digitizing the signals consists in their quantization both in time and amplitude and most important and informative characteristics of ADC are the speed and accuracy of conversion. The speed of conversion depends on the pass-band of their analogue part $[-F, F]$. In turn, most convenient and natural measure of the accuracy of digital estimates is the number of "true" – significant or "efficient" bits (ENOB [1]) in the output codes of estimates formed by an ADC. Before we discuss it, let us give minimal information about mathematical models used for the cyclic ADC description.

A. Mathematical models.

The mathematical model of the digital part of each CADC can be presented by the recurrent equation:

$$\hat{V}_k = \hat{V}_{k-1} + L_K \tilde{y}_k; \; (k = 1, ..., n), \tag{1}$$

where $\hat{V}_k$ is the code of the sample V (index m is omitted) in k-th cycle computed as a sum of the previous code $\hat{V}_{k-1}$ and digital observation $\tilde{y}_k$ formed by the N_{ADC}-bit pre-converter ADC_{In} in the analogue part of CADC. Values of the gains L_k in (1) depend on the type of CADC and parameters of the analogue part whose mathematical model can be satisfactorily well presented by the piece-wise linear transition function [4-10]:

$$\tilde{y}_k = \begin{cases} C_k(V - \hat{V}_{k-1}^{DAC} + v_k) + \xi_k & \text{for } C_k \mid e_k \mid \leq D; \\ D\text{sgn}(V - \hat{V}_{k-1}^{DAC} + v_k) + \xi_k & \text{for } C_k \mid e_k \mid > D, \end{cases} \tag{2}$$

which is an approximation of the commonly used ideal step-wise static transfer function. The analogue gain C_k in (2) may take different values depending on the number of cycle.

Value $\hat{V}_{k-1}^{DAC}$ in (2) represents the (formed by feedback D/A converter DAC_{In}) analogue equivalent of the estimate: $\hat{V}_{k-1} = E(V \mid \tilde{y}_l^{k-1})$ computed by the digital part of CADC in the previous cycle. Errors of D/A conversion can be included in the analogue noise v_k, which is a sum of the noise of the feedback chain, S&H block, subtractor Σ and possible external noise (below, we assume v_k is zero-mean white Gaussian noise with the variance σ_v^2). Parameter D in (2) determines the boundaries $[-D, D]$ of the full scale range (FSR) of ADC_{In}, and value ξ_k describes the quantization noise at the ADC_{In} output (its variance is denoted further as σ_ξ^2).

B. Differences between IC ADC and conventional CADC

The principal difference between IC ADC and usual CADC consists in the way of forming the output codes. In conventional CADC this operation is realized, in each

cycle, as repeated shifting and adding of observations $\tilde{y}_k$ to the upper bits of estimate $\hat{V}_{k-1}$ formed in the previous cycle. The number of bits in sequential estimates grows as $N_k = \Sigma_{i=1}^{k} (N_{ADC} - m_i)$, where m_k is the number of least significant bits (LSB) of the estimates $\hat{V}_{k-1}$ overlapped by the most significant bits (MSB) of the N_{ADC}-bit code $\tilde{y}_k$ shifted by N_{k-1} positions upwards, ($k = 1, \ldots, n$, $N_0 = 0$, $m_k = 1 \div 3$ bit). In IC ADC, each estimate has the same length of $N_{comp} >> N_k$ bits (3-5 bits greater than the required resolution of the converter). New estimate $\hat{V}_k$ is the sum of previous estimate and N_{comp}- bit word $L_k \tilde{y}_k$, ($k = 1, \ldots, n$).

Mathematically, this difference is reflected in the values of the gains L_k in (1). In conventional CADC these gains have the values from a narrow set of numbers [6]:

$$L_k = L_{k-1} 2^{-N_{ADC}+m_k} = L_1 2^{-N_{k-1}+m_k}. \tag{3}$$

In IC ADC, L_k may take arbitrary values from a practically continuous set of $2^{N_{comp}}$ binary words. The latter removes the obligatory, in CADC, limitations on the set of possible values of analogue gains ($C_k = L_k^{-1}$) and allows to set them, in IC ADC, to arbitrary permissible values. This is the key to constructing ICADCs which will be more efficient than any CADC realized with the same analogue elements.

C. Sources of superiority of optimal intelligent CADC over conventional ones [6, 8]

In a conventional CADC, the gains C_k of amplifier always have the values equal to reversed values of the gains L_k:

$$C_k = L_k^{-1} = L_1^{-1} 2^{N_{k-1}-m_k}. \tag{4}$$

In IC ADC, the gains C_k may take arbitrary values not violating the condition:

$$C_k = L_k^{-1}(1 - \gamma_k); \qquad 0 \leq \gamma_k << 1, \tag{5}$$

where γ_k is a stabilizing coefficient equal to zero in initial cycles of the conversion and to a small positive value after surpassing the threshold number of cycles. Single limitation to be kept is that gains C_k should have values excluding the appearance of converter's overloading. This can be easily arranged by setting the gains C_k, in each cycle of conversion, to the values satisfying statistical fitting condition [6, 10]. The latter condition determines the set Ω_k of permissible values of C_k which guarantee that the probability of CADC saturation does not exceed a given small value μ (depending on the requirements, this probability may have the value from the interval $10^{-12} \leq \mu \leq 10^{-3}$).

In IC ADCs, greater freedom in C_k setting allows to set these gains to the values somewhat greater than corresponding gains in conventional CADCs. This increases, in each cycle, the signal-to-noise ratio (SNR) at the pre-converter ADC_{In} output and improves the estimates in comparison with the estimates formed by conventional CADC. This is the first source of IC ADC advantage over CADC.

The second one is the possibility to search and set the gains C_k to the maximal permissible (optimal) values under given μ. Also, intelligent conversion allows to form the output codes employing sub-optimal adaptive signal-processing algorithms, which enable fast and most efficient suppression of ADC_{In} quantization noise (also correction of the input-output offsets, gains setting errors and non-linearities, as well as suppression of less influential analogue noise). It is important to notice that estimates formed by IC ADC are random values which reflect the influence of noise acting at the amplifier A input much more accurately than the estimates formed by the CADC.

The analogue parts of IC ADC and CADC of the same predestination are practically identical, and the difference concerns only their digital parts. From a technological point of view, the analogue part is the main part of a CADC which determines its complexity, size, power consumption and production costs, while the digital part necessary for implementation of a new conversion algorithm increases these parameters only by some percent.

3. RMS-BASED METHOD OF ENOB MEASUREMENT

The heuristic definition of the effective number of bits (ENOB) given in IEEE Standard [1], in our notation takes the form:

$$\hat{N}_k^{IEEE} = \log_2 \frac{FSR}{2\sqrt{3}RMS_k^{emp}}, \text{ where } RMS_k^{emp} = \sqrt{\hat{P}_k} = \sqrt{\frac{1}{M}\sum_{m=1}^{M}(V^{(m)} - \hat{V}_k^{(m)})^2}, \quad (6)$$

where $\hat{P}_k$ is an empirical analogue of the MSE of conversion errors $P_k = E[(V - \hat{V}_k)^2]$ after k cycles of conversion, and $RMS_k^{emp} = \sqrt{\hat{P}_k}$ is the empirical RMS. The value FSR describes the full scale (input) range of the CADC. As it was said in Sect. 2, for each $k = 1,...,n$, the set of possible values of estimates $\hat{V}_k$ in a conventional CADC is always discrete and consists of not more than $2^{N_{out}}$ numbers where $N_{out} = \Sigma_{i=1}^{n}(N_{ADC} - m_i)$ is the final resolution of the converter achieved after n cycles of conversion.

Our researches [4, 5, 7, 8] show a fast normalization of the conversion errors $\delta\hat{V}_k = V - \hat{V}_k$ for the greater number of conversion cycles. This effect is caused not only by the progressing, in sequential cycles, normalisation of the estimates $\hat{V}_k = V_o + \Sigma_{i=1}^{k} L_i \tilde{y}_i$ according to the central limit theorem but also by the growing influence of Gaussian noise v_k at the amplifier A input, when the conversion errors $V - \hat{V}_k$ take the values comparable with v_k.

Gaussian distributions of the input samples and of the values $\delta\hat{V} = V - \hat{V}_k$ allow to compute Shannon's amount of information in the estimates $\hat{V}_k$ about the input sample V [7, 8, 11, 12]:

$$N_k = I(V, \hat{V}_k) = H(V) - H(V/\hat{V}_k) = \frac{1}{2}\log_2\frac{\sigma_0^2}{P_k} = \log_2\frac{2\alpha\sigma_0}{2\alpha\sqrt{P_k}} = \log_2\frac{FSR}{2\alpha RMS_k}. \quad (7)$$

Values $P_k = E[(V-\hat{V}_k)]^2$ and $RMS_k = \sqrt{P_k}$ in (7) are the mean square error (MSE) and RMS of conversion errors, respectively. The value $FSR = 2\alpha\sigma_0$ represents the full scale range of the CADC. The saturation factor α is determined by the equation $F(\alpha) = (1-\alpha)/2$, where $F(\alpha)$ is a tabulated Gaussian error function. In turn, α determines the probability μ of CADC saturation (for instance, $\alpha = 5$ results in $\mu = 10^{-7}$). Being expressed in binary form, N_k represents the mean number of bits necessary for unambiguous presentation of the input sample values. For this reason it can be called also the effective number of bits – ENOB – of the estimates computed by IC ADC.

Comparison of (7) and (6) shows the closeness of these formulas. If the quantisation noise were Gaussian and numerical coefficients in the denominators had the same values ($\alpha = \sqrt{3}$), they could be considered as the analytical and empirical forms of expression for Shannon's amount of information determining effective number of bits in the estimates $\hat{V}_k$. However, PDF of quantization errors $\delta\hat{V} = V - \hat{V}_k$ in CADC and IC ADC is initially non-Gaussian and non-uniform due to the low resolution of pre-converter ADC_{In}, and takes the Gaussian form only at the end of the sample conversion. This means that bot formulas (6) and (7) wen used for the measurement of IC ADC performance, give initially non-accurate evaluations of ENOB. However, unlike (6), for the greater k formula (7) gives more and more realistic evaluations of ENOB that allows to use it for accurate final evaluations of IC ADC resolution. The empirical analogue of (7) enabling measurement of IC ADC ENOB has the similar form:

$$\hat{N}_k = \frac{1}{2}\log_2\frac{\sigma_0^2}{\hat{P}_k} = \log_2\frac{FSR}{2\alpha RMS_k^{emp}}, \text{ where } RMS_k^{emp} = \sqrt{\hat{P}_k} = \sqrt{\frac{1}{M}\sum_{m=1}^{M}(V^{(m)} - \hat{V}_k^{(m)})^2}. \quad (8)$$

Established by formulas (7), (8) the monotonic dependence between the ENOB and RMS shows that theoretically these measures are equivalent. However, in practical applications, so determined ENOB is a worse measure than RMS, because it implicitly realizes a non-linear transformation of inevitable errors in empirical estimates of RMS that increases the final level of ENOB evaluation errors. Also, as it was said above, formula (8) is not sufficiently adequate for evaluations at the initial stages of conversion. An additional shortage of (8) is that the results of its application depend on the form and distribution of the input signals.

Nevertheless, being a direct measure of the mean number of true bits in estimates formed by ADC (as well as by each digital measurement system), ENOB is a more

adequate, informative, clear and convenient for the analysis measure of conversion quality. Also important for the analysis is the shown above direct connection of the ENOB and information characteristics of the analyzed converters or measurement systems.

Let us note that formula (8) is accurate for the cycles near and after the "threshold" point n^* determined by corresponding general relationships [4-6], and gives only a rough evaluation of the ENOB in previous cycles. The necessity of more accurate estimation of ENOB values at the initial "pre-threshold" interval $[1, n^*]$ led us to the idea of direct measurement of ENOB using the concept of the first erroneous bit [4]. Below, we give a more accurate presentation of this measure and the approach to its measurement.

4. FIRST ERRONEOUS BIT (FEB) AND DIRECT MEASUREMENT OF ENOB

Let the codes $\hat{V}_k$ of the samples V be computed according to (1) by N_{comp}-bit processor. Then, let the computation error of each estimate $\hat{V}_k$ be not greater than $\Delta_{comp}/2$, where $\Delta_{comp} = FSR/2^{N_{comp}}$. In this case, the continuous set of the sample V values can be replaced, without loss of accuracy, by an the set of $2^{N_{comp}}$ discrete values $\hat{V}_k$, and both the samples and their estimates can be expressed by formulas:

$$V = \Delta_{comp}(j + 1/2) - \frac{FSR}{2} + V_0, \quad \hat{V}_k = \Delta_{comp}(\hat{j}_k + 1/2) - \frac{FSR}{2} + \hat{V}_0, \tag{9}$$

where j, $\hat{j}_k$ are corresponding numbers of quantization levels $(0 \le j, \hat{j}_k \le 2^N_{comp} - 1)$, V_0 is the centre of the input range of the CADC. It is assumed also that $\hat{V}_0 = V_0$. Formulas (9) allow to express the normalised error of conversion in the form:

$$\frac{err_k}{\Delta_{comp}} = \frac{|\, V - \hat{V}_k \,|}{\Delta_{comp}} = |\, j - \hat{j}_k \,| \, . \tag{10}$$

The binary presentation ($\text{mod}_2(.)$) of this error

$$\rho_k = \text{mod}_2\left(\frac{err_k}{\Delta_{comp}}\right) = \text{mod}_2 \,|\, j - \hat{j}_k \,|, \tag{11}$$

begins with a series of zeros which correspond to the "true", coinciding bits in the sample V and its estimate $\hat{V}_k$. The first unity in the binary word (11) determines the number of position where the first difference between the estimate and the sample appears. This position determines the number of "first erroneous bit" (FEB_k) in the code of estimate of the sample (further denoted as j_k^{FEB}) and the current number of "true" bits (NOB_k).

Definition 1. Number of true bits in the estimate $\hat{V}_k$ is determined by the formula:

$$\mathrm{NOB}_k = \mathrm{FEB}_k - 1 = j_k^{FEB} - 1. \tag{12}$$

Using so measured current values of NOB_k, one may measure the ENOB_k of IC ADC for each cycle of conversion (let us remind that values of the sample, its estimate and FEB are random values). The simplest way to determine ENOB is as follows:

Definition 2. ENOB of IC ADC is a low boundary of the set of M values of NOB_k obtained during conversion of M samples of the testing signal:

$$\mathrm{ENOB}_k = \min_{m=1,\ldots,M}(\mathrm{NOB}_k^{(m)}) = \min_{m=1,\ldots,M}[j_k^{FEB}(m)] - 1. \tag{13}$$

Formulas (11) – (13) directly show the method of measurement of the value of ENOB: one should convert M testing samples, find and collect the set of $\mathrm{NOB}_k^{(m)}$, $(m = 1, \ldots, M)$ using the corresponding FEB and, finally, use formula (13). The testing samples can be generated digitally and routed to the input of the CADC through N-bit D/A converter. The alternative testing method consists in applying the analogue signal to the inputs of IC ADC and a reference N_{comp}-bit A/D converter with further comparison of the codes formed by each of them.

An advantage of the proposed approach to ENOB measurement is its adequacy and simplicity. It does not depend on the form of testing signals and conditions of the experiment (at least for an ideal ADC) and can be easily implemented. It is also important that measurement of ENOB (13) does not require preliminary measurement of RMS or MSE. In Section 3 we wrote about difficulties in the ENOB (8) measurement caused by logarithmic transformation of RMS and MSE measurement errors, as well as about the dependence of numerical evaluations on the form and distribution of testing signals. Evaluations according to (13) exclude these dependencies. Below, some results of simulation analysis of the proposed approach are presented.

5. RESULTS OF SIMULATION ANALYSIS

The experiments were carried out using conventional (8) and new (13) definitions of ENOB. The IC ADC was modelled using the model (2) and sub-optimal algorithm described and studied in works [4-8]. The experiments were carried out under the following parameters: $N_{ADC} = 4$, $N_{DAC} = 12$, the variance of the analogue noise $\sigma_v^2 = 6.25 \cdot 10^{-10}$, $FSR = [-1, 1]$, $M = 10000$. The ramp full-scale-range testing signal was used.

Estimated typical distributions of the frequency of FEB appearance in different positions of the code of estimates $\hat{V}_k$ in sequential cycles of conversion ($k = 1, 2, 3, 4$, plots from left to right) are presented in Fig. 2. The plots have a complex form which

depends on the number of conversion cycles. There is a well seen appearance, for the greater cycles, of a small but noticeable number of FEBs preceding the main peak of FEB appearances.

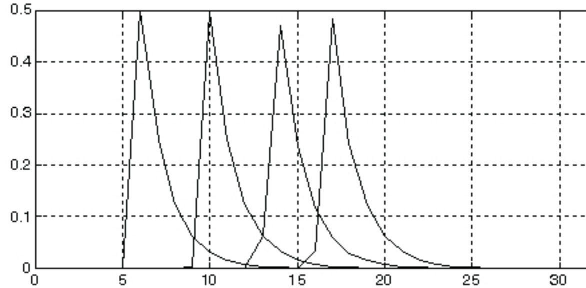

Fig. 2. Histogram of the FEB appearance in initial (k = 1, 2, 3, 4) cycles of conversion.

The plots in Fig. 3 show the changes of PDF (probability density function) (Fig. 3a) and CDF (Cumulative distribution function) (Fig. 3b) of FEB occurrences in different position of the codes $\hat{V}_k$ depending on the number of cycles. Figure 4 presents different sections of the surface formed by the histograms of ENOB presented in Fig. 3a. Figure 4a is the view from the top, and Fig. 3b,c show the distribution of FEBs in regions where FEB appeared at least three times and at least once, respectively.

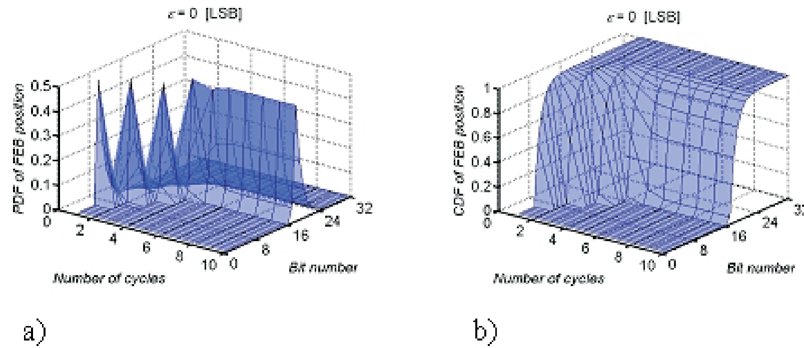

Fig. 3. Changes of: (a) histogram of frequency and (b) probability of FEB appearance in first ten cycles of conversion (experiments with sub-optimal IC ADC).

Intensity of grey in Fig. 4a refers to the more frequent FEB occurrences; grey area in Figs. 4b, c corresponds to positions where the number of FEB occurrences is greater than a given value. The continuous line in Fig. 4c refers to ENOB assessed using formulas (8) (non-direct method). One can see a large number of well-estimated

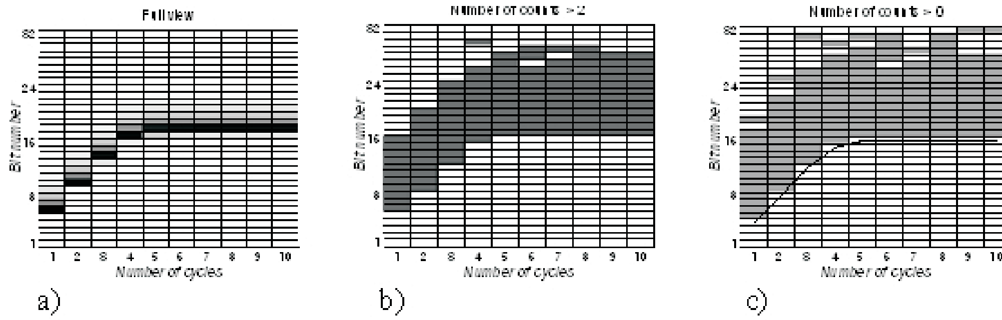

Fig. 4. Evolution of histogram of FEB appearance: (a) view from the top and (b), (c) – regions where FEB appeared at least three times and at least once, respectively [7].

samples (FEB appears in positions even higher than the twentieth). This is a result of noisy effects which makes us think that the measure (13) can be too restrictive. This question deserves a deeper analysis.

There was carried out also initial simulation analysis of capability of ENOB (13) to reflect the influence of INL and DNL on the resolution of IC ADC. The results of conventional and direct measurement of ENOB under different values of DNL and INL of ADC_{In} are shown in Figs. 5 and 6. DNL errors of ADC_{In} were modelled as independent random (distributed uniformly) displacements of ADC_{In} quantization thresholds around their nominal values. The width of the interval ε [- $\Delta_{ADC}/2$, $\Delta_{ADC}/2$] of possible displacements was set using the scale ("intensity") coefficient ε (value Δ_{ADC} describes the ADC_{In} quantization interval).

INL errors of ADC_{In} were modelled, similarly as in [13], by replacement of the linear approximation of ADC_{In} transfer function by a function of the $x^{1+\lambda}$ type where λ determines the intensity of INL errors:

$$f(x) = D\mathrm{sgn}(x)\left(\frac{|\,x\,|}{D}\right)^{1+\lambda}. \tag{14}$$

Dependencies on the number of cycles of the changes of FEB distribution due to DNL and INL errors for $\varepsilon = 0.05$ and $\lambda = 0.05$ [LSB], respectively, are presented in Figs 7 and 8. Continuous lines in Figs 7c and 8c refer to ENOB assessed using the conventional non-direct approach (8). The results presented in Figs 7 and 8 coincide with the results in Figs 5 and 6.

The results of analysis allow us to conclude that the results of ENOB evaluation obtained by the direct method (FEB-based ENOB measurement) are somewhat more pessimistic than those obtained by the conventional method. This can be explained in the following way.

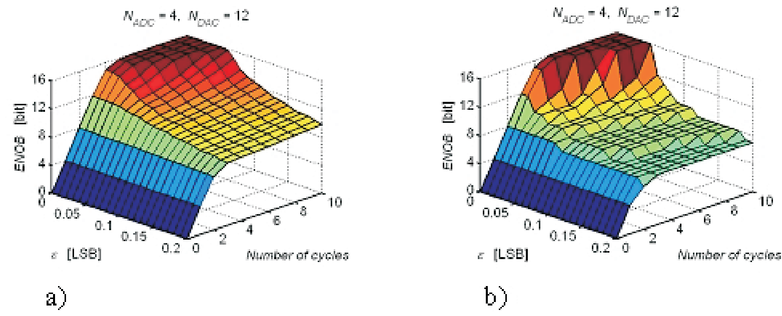

Fig. 5. Influence of DNL of ADC_{In} on the ENOB measured using: (a) conventional and (b) FEB-based approach.

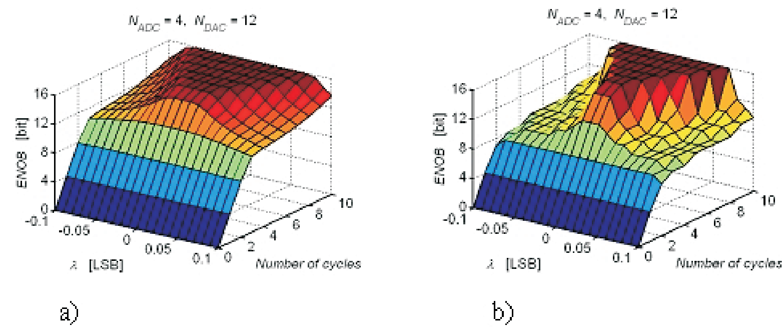

Fig. 6. Influence of INL of ADC_{In} on the ENOB measured using: (a) conventional and (b) FEB-based approach.

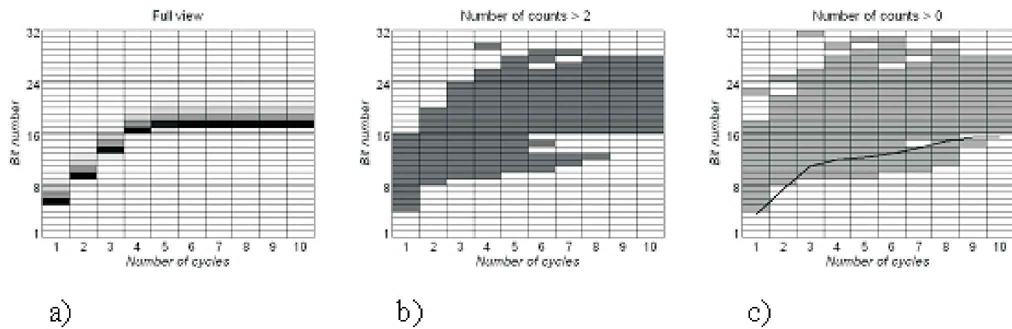

Fig. 7. Evolution of histogram of FEB appearance in case of DNL errors for $\varepsilon = 0.05$: (a) view from the top and (b), (c) – regions where FEB appeared at least three times and at least once, respectively.

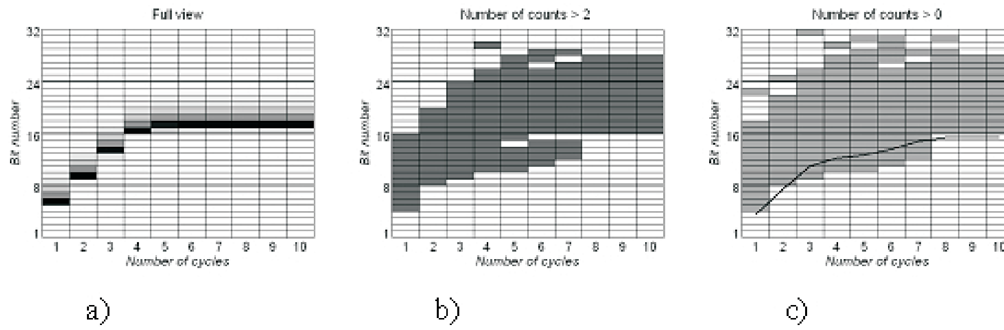

Fig. 8. Evolution of histogram of FEB appearance in case of INL errors for $\varepsilon = 0.05$: (a) view from the top and (b), (c) – regions where FEB appeared at least three times and at least once, respectively.

RMS-based ENOB assessed according to (8) is less sensitive to INL and DNL errors of the internal converter ADC_{In} of IC ADC, which during conversion of some samples cause the saturation of ADC_{In} and appearance of abnormal errors of conversion. The influence of a small amount of abnormal errors is diminished by averaging of a large number of errors during calculation of RMS. Thereby, we neither receive adequate information about "normal" IC ADC performance quality nor about abnormal errors, because these two types of errors are mixed.

In turn, direct evaluation of FEB-based ENOB is sensitive to appearance of singular abnormal errors, because it gives the value of ENOB equal to the number of true bits in the worst estimate among all output codes.

However, as it was said above, the final choice of the adequate measure remains yet an open question requiring additional study of statistical characteristics of FEB and NOB.

6. CONCLUSIONS

The results of investigations show that the direct FEB-method of CADC ENOB measurement is a perspective and inherently more adequate tool for assessment and analysis of IC ADC performance. An important feature of the FEB-based approach is that it allows, in perspective, to separate regular performance characteristic and rare abnormal errors. Its further development may yield a universal, convenient and adequate method of ADC testing.

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